"Andes OBC": a COTS-Based On-Board Computer for Small Satellite Missions

Sebasthian Ogalde[a], Eduardo Novoa Carrasco[b], Ilaria Merli[c] , Jorge Olmos[d] , Carlos E. González[e]

[a] Andes Aerospace, Chile. Email: sebasthian.ogalde@andesaerospace.cl,
[b] Andes Aerospace, Chile. Email: eduardo.novoa-externo@andesaerospace.cl
[c] Andes Aerospace, Chile. Email: ilaria.merli-externo@andesaerospace.cl
[d] Andes Aerospace, Chile. Email: jorge.olmos-externo@andesaerospace.cl
[e] Departamento de Ingeniería Informática, Universidad de Santiago de Chile, Santiago, Chile Email: carlos.gonzalez.c@usach.cl

ABSTRACT

Andes OBC is an onboard computer (OBC) for CubeSat satellite missions built on commercial off-the-shelf components (COTS). A core feature of its design is full redundancy of every component, implemented to significantly enhance operational reliability. Based on the Arm Cortex-M7 microprocessor, it is capable of handling the operations of nanosatellites of various form factors, from 1U to 6U CubeSat platforms. These operations include: power management, input/output (I/O) processing, telemetry and telecommand (TM/TC) from and to Earth stations, and satellite payload management, which can include an artificial intelligence (AI) algorithm to optimize its operations. In this work, the main design drivers and characteristics are reviewed, and a series of tests successfully conducted on some of the peripherals used to evaluate the proposed OBC architecture are presented.

Introduction

The CubeSat concept, which had its inception in the year 2000 [1], has emerged as a market that has experienced significant growth in recent years, driven by decreasing launch costs and increasing demand for diverse applications ranging from Earth observation and remote sensing, to scientific research and communication constellations. This proliferation of small satellites has created a need for increasingly capable on-board computers (OBCs) to manage complex tasks, handle larger volumes of data, and enable more autonomous operations.

Traditionally, space-grade components have been used in OBC designs to ensure reliability in the harsh space environment. However, these components are often expensive and have considerable lead times. The use of commercial off-the-shelf (COTS) components offers a compelling alternative, providing cost-effectiveness and faster development cycles. This paper presents the design and development of a novel, modular OBC architecture based on COTS components and incorporated artificial intelligence (AI) capabilities for serving a wide range of small satellite missions.

This design has been done by our company Andes Aerospace, based in Chile. To the best of our knowledge, this marks a significant step as it represents the first instance of a privately developed on-board computer specifically designed and intended for commercial applications in the small satellite sector. This initiative underscores the growing maturity of the private space industry and the increasing role of commercial entities in providing critical hardware for space missions.

The accessibility and cost-effectiveness of CubeSats has opened doors for emerging space programs in developing countries. These nations are leveraging CubeSat technology to pursue their own space ambitions and goals. For example, initiatives like the SUCHAI program in Chile have demonstrated the potential of CubeSats for fostering space research and development in emerging economies [2]. These programs not only contribute to scientific knowledge but also play a crucial role in building local expertise and capabilities in the space sector.

Design Drivers

In space system design, especially for mission-critical subsystems such as On-Board Computers (OBCs), having a well-defined set of design objectives, requirements and constraints is essential to ensure that the final implementation meets functional, operational, and environmental expectations. These design criteria serve as the foundation for both the system architecture and the verification process. In the case of the Andes OBC, the criteria were derived mainly from three different mission profiles: research projects using CubeSats, commercial low-cost satellite constellations, and general payload data processing.

Therefore, a key design driver for this OBC is the flexibility to support various satellite form factors, from 1U to 6U CubeSat platforms. . The Andes OBC is designed with customisability and scalability in mind, to function not only as the primary spacecraft controller but also as a dedicated payload controller when needed. Additionally, the characteristics of the deployment environment (e.g., LEO orbit), and the need for compatibility with other satellite subsystems serve as an additional design driver and constraint for Andes OBC's electronic components and communication interfaces.

Requirements definition

The Andes OBC project is guided by a requirements-driven development methodology designed to ensure mission readiness, platform compatibility, and long-term maintainability. At its core lies a carefully structured set of system requirements, formally defined to address the needs of modern small satellite missions operating in constrained and dynamic environments. These requirements not only shape the system's architecture, but also enable a scalable and verifiable integration path for diverse use cases.

From the outset, the Andes OBC was conceived to operate in Low Earth orbit (LEO), a context that imposes specific constraints in terms of environmental exposure, communication protocols, and energy availability. As a result, the system level requirements reflect essential operational domains such as radiation tolerance, energy efficient processing, subsystem interoperability, and autonomous fault recovery. These requirements were derived from a mission profile that anticipates high reliability and adaptability in compact satellite platforms, particularly those adhering to CubeSat standards.

To support both development and deployment, the Andes OBC adopts a hierarchical classification of requirements. This structure ensures traceability between stakeholder goals, functional capabilities, and technical implementations. High-level requirements are mapped onto concrete hardware and software specifications. This alignment allows for clear validation strategies and minimizes the risk of integration bottlenecks later in the development cycle.

The verification strategy is designed to be incremental and traceable. Each requirement is explicitly linked to corresponding test procedures, ranging from interface validation to functional behavior under nominal conditions and/or failure modes.

The system undergoes structured validation stages across multiple hardware and software versions, enabling continuous refinement while preserving design intent. This approach not only supports confidence in mission-critical functionality, but also demonstrates readiness for integration into diverse satellite architectures.

System Level Requirements

System-level requirements define the fundamental functional and operational capabilities that the Andes OBC must fulfill in order to support mission success.

1. **Environment & Radiation:** The Andes OBC is intended for deployment in Low Earth Orbit (LEO), where it will be exposed to varying levels of radiation and temperature fluctuations. As such, the system must ensure reliable operation under radiation effects such as Single Event Upsets (SEUs) and Total Ionizing Dose (TID).
2. **Processing Power and Artificial Intelligence:** This group of requirements addresses the need for sufficient computational performance and memory throughput to support advanced onboard processing. In particular, the Andes OBC is expected to enable AI-driven functionalities such as autonomous decision-making and data filtering. These capabilities aim to reduce data transmission demands and improve spacecraft autonomy during mission operations.
3. **ADCS & GNSS:** Although not intended to serve as a full Attitude Determination and Control System (ADCS), the Andes OBC must offer baseline support for orientation-related tasks. This includes the ability to process data from inertial and magnetic sensors, and optionally, to interface with Global Navigation Satellite System (GNSS) modules. These functions contribute to enhanced spacecraft awareness and basic control strategies.
4. **Onboard Memory:** Reliable onboard storage is critical for both system operation and mission data retention. Requirements in this category define the expected memory architecture, emphasizing redundancy, non-volatility, and data integrity. The OBC must ensure persistent storage of firmware and telemetry, with a mechanism to tolerate faults such as bit-flips caused by radiation.
5. **Launch and Operations:** This category of requirements ensures that the Andes OBC can handle the transitions and operational events associated with the launch sequence and in-orbit operation. Key aspects include autonomous boot-up behavior, fault recovery modes, and safe-state transitions. These

features are vital to maintaining system stability and mission continuity.

6. **Internal Communication:** Internal communication requirements define how the OBC interfaces with other subsystems within the satellite. The system must be compatible with standard protocols used in CubeSat architectures, enabling seamless integration and coordination with subsystems like power management, ADCS, and payload controllers.
7. **External Communication:** Although external communication hardware (e.g., radios) is managed by other subsystems, the Andes OBC must support integration with them. This includes handling of telemetry, telecommand packaging, and synchronization with communication events, ensuring data is correctly formatted and delivered for ground interaction.
8. **Development & Testing:** These requirements focus on ensuring the Andes OBC can be effectively developed, validated, and maintained. This includes provisions for debugging, software updates, and functional testing interfaces, all of which are essential for efficient iteration and long-term reliability.
9. **Regulatory:** To ensure compliance with deployment constraints, the OBC must meet mechanical, electromagnetic, and safety standards applicable to CubeSat missions. These requirements contribute to flight readiness and compatibility with launch providers and satellite deployers.

OBC Characteristics

Andes OBC's characteristics are a direct result of the definition of System Level Requirements abovementioned. These characteristics enable the selection of components that cover the expected functionality. The selection of COTS components was carefully considered, prioritizing factors such as processing power, power efficiency, availability, cost, and inherent radiation tolerance.

Processing power and memory

While specific part numbers are not disclosed due to commercial sensitivity, the OBC utilizes a 32-bit ARM Cortex-M class microprocessor known for its low power consumption when configured with low processor frequencies, and its flexibility to also process data with robust performance. Another advantage of using this architecture is its compatibility with freely available compilation tools such as the ARM GNU Toolchain based on GCC, well-known Real-Time Operating Systems (RTOS) such as FreeRTOS, low-cost debugging interfaces, which allows the user to quickly prototype and test their own applications.

A critical element of a CubeSat's On-Board Computer (OBC) is its memory subsystem, engineered to reliably manage mission data and execute flight software. These subsystems strategically combine volatile and non-volatile memory types to guarantee data integrity under challenging conditions and provide adequate storage capacity for mission duration. The Andes OBC implements this strategy with specific component choices: it utilizes NAND Flash memory as its high-capacity, non-volatile mass storage. This is primarily designated for storing large datasets, such as scientific instrument readings from payloads, system logs, and configuration files that need to be preserved reliably. Complementing this, the Andes OBC employs 2MB of Magnetoresistive RAM (MRAM) to function as its main operational memory. This MRAM handles the demands of real-time processing, serving as the workspace for code execution and temporary data storage, benefiting from its RAM-like speed coupled with inherent non-volatility for enhanced robustness against power interruptions or radiation events.

Sensors

To gather essential data regarding its operational environment and physical state, the Andes OBC is equipped with a dedicated set of external sensors. This includes strategically placed external temperature sensors designed to monitor thermal conditions at various critical points on the CubeSat structure. For comprehensive motion and orientation sensing, the OBC interfaces with a high-accuracy, 6-axis Micro-Electro-Mechanical System (MEMS) Inertial Measurement Unit (IMU). This sensor provides precise measurements of both linear acceleration and angular velocity, crucial for tracking the satellite's dynamics. Complementing the IMU, particularly for attitude determination, is an ultra-low-power, 3-axis digital output magnetometer. This sensor measures the ambient magnetic field vector with precision, aiding in orientation calculations relative to Earth, while its ultra-low power characteristics minimize the drain on the satellite's power budget. Together, these sensors provide vital inputs for spacecraft health monitoring, thermal control, and a basic Attitude Determination and Control System (ADCS).

Communication

The Andes OBC is designed with a versatile suite of communication interfaces to ensure compatibility with a broad range of nanosatellite subsystems and payloads currently present in the market. It incorporates standard protocols: UART, I2C, SPI, and CAN. UART is used

for basic serial communication. I2C allows for connecting multiple low-speed peripherals like sensors and payloads. SPI offers higher-speed serial communication for devices like flash memory, meaning that external memories can be added by the user to Andes OBC. CAN is a robust, message-based protocol suitable for critical communication between subsystems. These interfaces enable seamless integration and flexibility in mission design, and some of them are fully compatible with the CubeSat Space Protocol.

The use of the CubeSat Space Protocol library (libcsp) [3] is considered as a significant design driver for the communication interfaces of the Andes OBC. Libcsp is a lightweight network protocol designed specifically for CubeSats, offering features like reliable packet delivery, routing, and network management within a resource-constrained environment. By incorporating the libcsp, the Andes OBC aims to ensure robust and efficient communication between its internal subsystems and with external entities such as ground stations or other satellites. This choice aligns with the need for interoperability and standardized communication practices in the CubeSat community.

Radiation mitigation and Redundancy

A critical challenge when using COTS components in space applications is mitigating the effects of radiation. This OBC design addresses this challenge through a multi-layered approach. First, components with inherently higher radiation tolerance within the COTS category were prioritized. Second, shielding techniques are employed to protect sensitive components from total ionizing dose (TID) effects. Finally, software-based mitigation techniques, such as error detection and correction (EDAC) codes, are implemented to detect and correct single-event upsets (SEUs) and other radiation-induced errors.

To provide protection against the space environment, the OBC includes an aluminum shield with a defined thickness that compromises between shielding performance and mass compliance.

A cornerstone of the Andes OBC design philosophy is the maximization of operational reliability and mission resilience through a comprehensive redundancy strategy. This is achieved by implementing full duplication of critical hardware components and subsystems. Specifically, the architecture features two identical main processing cores (Arm Cortex-M7), ensuring that processing capabilities are maintained even if one core experiences a failure. This duplication extends to the memory systems, with complete replication of both the operational MRAM and the non-volatile NAND Flash mass storage, safeguarding critical flight software, operational data, and stored payload information. Furthermore, key onboard sensors, such as those used for attitude determination (like IMUs and magnetometers), are included in redundant pairs. Essential communication interfaces, responsible for vital telemetry, telecommand (TM/TC), and potentially other data links, are also fully duplicated. This 'two-of-everything' approach significantly enhances fault tolerance, allowing the OBC to potentially switch to the backup component or subsystem seamlessly in the event of a failure in the primary unit.

Mechanical

The mechanical constraints of the Andes OBC are defined to ensure full compatibility with CubeSat form factors and deployer interfaces. These requirements address dimensional limits, mass budgets, structural considerations, and mechanical integration. Each aspect has been explicitly defined to support seamless satellite integration while minimizing development risk. Following that constraint, Andes OBC follows the PC/104 standard [4].

This standard defines a compact, stackable form factor and bus architecture derived from the industry-standard PC ISA bus. PC/104 is particularly well-suited for embedded systems and applications requiring ruggedness and small size, making it appropriate for CubeSat applications. By adhering to the PC/104 standard, the Andes OBC ensures mechanical compatibility and ease of integration with other PC/104-compliant boards, allowing for modular expansion and customization of the satellite system.

Software

To further enhance the reliability and robustness of the Andes OBC, we have incorporated and adapted key elements from the flight software developed for the successful SUCHAI series of CubeSats by the University of Chile [5]. The SUCHAI missions –SUCHAI 1, 2, 3, and PlantSat– have demonstrated consistent and successful operations in orbit [6], validating the reliability of their flight software. By leveraging this proven software base and modifying it for the specific hardware and mission requirements of the Andes OBC, we aim to benefit from the existing flight heritage and minimize potential software-related risks. This approach significantly increases confidence in the Andes OBC's operational stability and reduces the development cycle time by building upon established and validated code.

Experimental Test Plan

Testing is a crucial step for the Andes OBC (On-Board Computer) designed for nanosatellites. As a critical component responsible for managing satellite operations, the Andes OBC must undergo rigorous validation and verification to ensure its reliability in the harsh space environment.

The test plan for Andes OBC encompasses software, hardware, and mechanical tests, as well as system-level and environmental validations such as thermal vacuum (TVAC) and vibration testing. These comprehensive tests are essential to verify the OBC's functionality, durability, and performance under various conditions, ultimately ensuring the success of satellite missions and the integrity of collected data.

Each item of the development of Andes OBC will be tested individually. Given the unit-module nature of Andes OBC, every test will indicate univocally which item is under test.

In order to split the complexity of the OBC and to speed-up the first hardware developed, we have decided to develop the OBC in successive versions. Each version is built over the previous one, and allows us to focus and test some functions needed by the final OBC. As a first approach, we considered two main versions to be enough, v1 and v2, where the latter should include all the required functionality of the OBC. The versions mentioned include:

1. **Andes OBC v1**:
    a. board with one processor. No redundancy.
    b. Interfaces available: UART, I2C, SPI, CAN, PWM, GPIO and ADC.
    c. Memories available: External RAM (MRAM), mass memory (NAND), microSD card socket.
    d. External sensors available: temperature
    e. PC104 connector with preliminary pin availability.
2. **Andes OBC v2 (final)**:
    a. Full redundancy on: sensors, memories, processor.
    b. External sensors available: temperature, IMU, magnetometer.
    c. External watchdog
    d. PC104 connector with final pin availability.

Andes OBC development is foreseen to be completed in July 2025. At the moment of writing, Andes OBC v1 has been fully developed and partially validated. A non-comprehensive list of tests and their objectives are listed in Table 1.

Title of test	Objective of test
Temperature read using I2C	Validate temperature reading using external sensor connected through I2C.
SPI read/write	Validate SPI communication (send/receive) using an externally connected board through SPI.
NAND read/write	Validate external NAND memory read/write operations.
Sleep and Wake-up on pin	Validate hardware configuration for Sleep, and Wake-up on pin reading through interrupt.
CAN	Minimal test for 2x CAN interfaces read/write.
MRAM	Validate external MRAM read/write operations.
Real time clock (RTC)	Validate RTC hardware configuration and on-board hardware coin-cell battery connection.
PWM Generation	Validate PWM generation using internal timers.

Table 1: Non-comprehensive list of tests to be performed on Andes OBC v1.

Testing Procedures

For each test an individual testing procedure has been written. Each testing procedure is composed of the following parts:

1. **Title and test number**: self-explanatory.
2. **Description**: brief description and objective of the test.
3. **Requirements covered**: every test procedure must be tied to a specific list of requirements that are being validated by the test.
4. **Materials needed**: comprehensive list of materials needed to perform the test, including hardware, software, and any other tools that are required.
5. **Testing conditions**: this is a description of the starting conditions of the test. For example,

how the Andes OBC must be connected to a specific tool such as an oscilloscope or logic analyzer, and which programs need to be open and ready on the working station.

6. **Pass/fail criteria**: Pass/fail criteria in a test are the specific conditions that must be met for the test to be considered successful (pass) or unsuccessful (fail). These criteria define what constitutes an acceptable outcome and provide a clear benchmark for evaluating the results of the test.
7. **Test steps**: this section includes detailed, sequential instructions that outline how to perform a specific test. They provide a clear, step-by-step procedure to follow, ensuring consistency and repeatability in the testing process. Each step describes a specific action to be taken by the test operator, along with any expected inputs or observations.

Test Results

The tests were executed in our premises in Antofagasta, Chile. The final test results are summarized in Table 2.

Title of Test	Test Result
Temperature read using I2C	PASSED.
SPI read/write	PASSED.
NAND read/write	PASSED.
Sleep and Wake-up on pin	PASSED.
CAN	PASSED.
MRAM	PASSED.
Real time clock (RTC)	PASSED.
PWM Generation	PASSED.

Table 2: Test results, on tests performed on Andes OBC v1.

Conclusions

We have presented the main design drivers of Andes OBC, its main system requirements and the resulting chosen components and characteristics, taking into account processing power, power efficiency, availability, cost, and inherent radiation tolerance.

The successful completion of basic validation for the Andes OBC v1 marks a significant initial milestone. This phase, encompassing integrated tests of hardware components and their corresponding software drivers, confirms the viability of the core design and establishes a robust foundation for subsequent development. It demonstrates that the fundamental interaction between the selected hardware and the low-level software is functional, reducing risks associated with the core architecture as the project progresses towards a more complex, flight-ready system. This validated baseline provides essential groundwork and confidence for moving forward towards the next version of Andes OBC: v2. This involves both the concluding development tasks and the procurement of necessary components for the upgraded version v2.

The planned testing and validation of new on-board sensors, specifically the Inertial Measurement Unit (IMU) and magnetometer, are crucial. Integration of these sensors directly implies the potential for Attitude Determination and Control System (ADCS) functionality within the CubeSat. Another aspect present in Andes OBC v2 is testing the inter-processor communication architecture that is directly linked to implementing redundancy within the OBC. This is a critical feature for enhancing system reliability and fault tolerance.

The final integration of the SUCHAI flight software stack with the hardware drivers represents the culmination of the development effort. This step moves beyond basic driver verification to enabling the full suite of intended OBC functionalities – managing subsystems, executing autonomous operations, handling complex data flows, implementing communication protocols, and running the specific mission logic defined in the SUCHAI software. By utilizing and adapting existing, flight-proven software from the SUCHAI missions, the Andes OBC project fosters collaboration and knowledge transfer within the national space sector.

Acknowledgments

This work was funded by the National Agency for Research and Development (ANID), STARTUP CIENCIA/2024 - SUC240027.

Bibliography

1. H. Heidt, J. Puig-Suari, A. Moore, S. Nakasuka, and R. Twiggs, "CubeSat: A new

generation of picosatellite for education and industry low-cost space experimentation," in *Proc. AIAA/USU Conf. Small Satellites*, Logan, UT, USA, Sep. 2000.
2. M. A. Diaz, J. C. Zagal, C. Falcon, M. Stepanova, J. A. Valdivia, M. Martinez-Ledesma, J. Diaz-Pena, F. R. Jaramillo, N. Romanova, E. Pacheco, M. Milla, M. Orchard, J. Silva, and F. P. Mena, "New opportunities offered by Cubesats for space research in Latin America: The SUCHAI project case," *Adv. Space Res.*, vol. 58, no. 10, pp. 2134-2147, Nov. 2016.
3. libcsp, "[libcsp]," GitHub, Available: https://github.com/libcsp/libcsp, Accessed: Apr. 15, 2025.
4. PCI/104-Express™ & PCIe/104™ Specification. Including OneBank™ and Adoption on 104™, EPIC™, and EBX™ Form Factors. Los Gatos: PC/104 Consortium, 2015. Rev 3.0.
5. C. E. Gonzalez, C. J. Rojas, A. Bergel, and M. A. Diaz, "An architecture-tracking approach to evaluate a modular and extensible flight software for CubeSat nanosatellites," *IEEE Access*, vol. 7, pp. 126409-126429, Oct. 2019.
6. C. Garrido, E. Obreque, M. Vidal-Valladares, S. Gutierrez, M. Diaz Quezada, C. Gonzalez, C. Rojas, and T. Gutierrez, "The First Chilean Satellite Swarm: Approach and Lessons Learned," in *Proc. AIAA/USU Conf. Small Satellites*, Logan, UT, USA, Aug. 2023.