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Radiation hardened single chip true digital Sunsensors and their development path.

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Abstract:

True digital Sunsensors (albedo insensitive and with a digital interface) have been under investigation by ESA since the 1990's. 2024 however is the first year that the silicone required to produce a single chip radiation hardened true digital Sunsensor has been delivered to Lens R&D B.V.

Once fully functional, this single silicone chip (size 5.5*6.5 mm^2) is expected to be a game changer for Sun attitude measurement applications.

This paper will describe the various aspects of the chip design test status and expected development path.

As the program is progressing at a high pace, the presentation at the conference might include a bit more data, but this paper describes the situation as is in the beginning of April 2025.

Design requirements.

In frame of the ARTES program at hand, ESA only posed a very limited number of requirements. The preliminary requirements are given in Table 1.
Based on these requirements a silicon chip has been designed that should be able to fulfill the majority of these requirements.

Deviating from these requirements have been mainly agreed upon because the main requirement was to build a solution that could be sold for less than 20k€/units @ 6 pcs.

This requirement calls for a sensor that is optimized for volume production and de-complicated to the largest extend possible.

Fortunately, a lot of pre-developments have been done between 2004 and 2010 by TNO as reported in [AD-01] so the design could start on basis of a lot of background knowledge available.

Fields	Requirements	Specification	Verification
Functional	Output	Sun direction in SC frame	R, T
Performance (over full thermal & dynamics environment)	Angular accuracy (including tolerance to solar flares, SEU, albedo and stray light)	- Over full FOV: 5° (3 sigma) - Over accurate FOV: 1° (3 sigma) (target 0.5°)	R, A, T
	Field Of View full cone	- Full FOV: Hemisphere - Accurate FOV: +/-30°	R, A, T
Interfaces	Full system Mass	400 g	R, A, T
	Sensor Dimensions (without electronic)	120 x 120 x 60 mm	R, A, I
	Electronics Dimensions (if deported)	100 x 100 x 50 mm	R, A, I
	Average power consumption	2 W	R, A, T
	Average power dissipation	2 W	R, A, T
	Thermal accommodation	No radiator shall be used	
	Supply voltage	5V regulated OR 12V OR 28V OR 50V unregulated	R, A, T
	Data interfaces	Digital: type TBD	R, A, T
Design and PA	Redundancy	Internal	R, I, T
	Lifetime	15 years in GEO	R, A
	Thermal cycles	7000	R, A
	Reliability	100 FIT @ 30°C	R, A
	Radiation	-Electronic components: 100Krad -Optics: 300 Krad -Detector if any: 1 Mrad -SEU tolerant	R, A
	No ITAR components	ITAR free	R
Environment	Dynamics	Angular rate: +/- 100°/s	R, A
	Temperature	-Storage and operational: -40 to +75°C -Extension for Solar Array accommodation: -80 to +100°C (TBC)	R, A, T
	Vibration and shocks	-Sine: 20 g peak -Random: 27 g rms -Shock: 3000g from 2 to 10kHz	R, A, T

Note that the verification methods are associated to a letter:

- R: Review of design
- A: Analyses
- T: Tests
- I: Inspection

Table 1 DSS requirements

Implementation

The one relevant requirement not stated is Table 1 is a target price of <20k€/sensor @6 pcs.

This target price in combination with the requested reliability of 100FIT@30°C more or less mandates the use of a single silicon chip (no additional active circuits) and no Christal oscillator (as a high reliability Christal oscillator can easily soup up half of that budget).

Second important parameter to take into consideration is the overall power dissipation. This parameter is important and should be optimized to the largest extend possible because a Sunsensor not only needs to operate in vacuum but will also be facing the Sun directly preferably without any requirements on using multi-layer Isolation blankets (MLI) or external secondary surface reflectors or radiators (the later is a formal requirement). Reducing internal power dissipation and minimizing absorption of solar radiation therefore have been a key priority so far, and will be a key priority in the future.

Small sensor size in that sense not always helps, as it will reduce the amount of absorbed solar energy, but it will also decrease the contact area with the spacecraft, thus limiting the potential for heat transfer.

During the design phase it was demonstrated that the majority of power dissipation is associated with the data interface and supply voltage reduction. As most of the power consumption was associated with the data interface, a careful selection of an appropriate interface has been performed.
After an extensive analysis of all available space qualified interfaces, it was concluded that none of them were fit for interfacing to a single chip digital Sunsensor. As a result, a dedicated interface was selected.

Due to the low speed, low power and a-synchronous character of an SPI interface, this standard was chosen to interface to the Sensor.

To avoid issues during EMC testing and increase the reliability of data communication, a differential interface was opted for. To avoid the dissipation associated with the termination resistors, all termination resistors are projected to be placed at the spacecraft computer side.

The second largest power dissipation source is the supply voltage reduction required. The produced chip operates at 3.3V externally, but mainly uses 1.8V circuits for the digital part. As a result, the overall power dissipation is determined by the operating current required times the supply voltage. Using a 5V supply voltage to supply a sensor core that is running at 1.8V, means a power efficiency of some 30% (60% is wasted by producing heat) Adding a DC/DC converter can improve on this efficiency but not very much for very low powers. In addition, adding a DC/DC converter adds complexity, EMC related issues and costs.

By de-sensitizing the detector for supply voltage variations it has shown to be possible to generate a sensor that can operate over a wide range of input voltages but operating a good quality imager at 1.8V only was not seen as feasible. It would have been possible to lower the power dissipation even further by adding a second external power input (for the 1.8V circuits) but despite this potential gain in power efficiency for the sensor it has been decided to include a low drop-out power regulator on chip so as to be able to supply the entire sensor from a single power supply (>2.5V..<3.6V) . This reduces complexity of the external interfaces at the cost of a higher power dissipation, but is still expected to be the optimum solution at system level.
By optimizing the power consumption to be as constant as possible (assisted by the differential SPI interface for instance) it is expected that a simple RC filter on the input of the circuit will allow to filter the input voltage to such an extent, that neither emitted radiations nor radiated or conducted susceptibility requirements generally posed to electronics will be an issue.

To complement the chip commonly used features like a slow start circuit, watchdog timer, latching current limiter (LCL) and low drop-out regulators (LDO) are all implemented on a single chip.

For the testbed several additional decoupling capacitors have been foreseen which should not be necessary for the final circuit as well as some selection straps that can be used to select different modes of operation for the chip. The total has resulted in a testbed design as shown in Figure 1.

To the right there are the serial clock (SCLK) Data-IN (MOSI) and Data-out (MISO) lines as well as the single 3.3V power input to which a simple RC filter is connected. As with the BiSon sensors, a 1.2MΩ±20% resistor will be used to connect the floating circuit to the case to avoid electric charging.

A solderable strap will allow for a single ended or differential SPI interface (SPI-config). Two more straps will allow to disable the LDO and LCL in case those circuits would prove to be non-functional and a single capacitor is required to stabilize the 1.8V LDO. A strap is implemented on the chip allowing to bypass the LCL and feed the chip directly from primary input power. A single reference current resistor is implemented biasing the entire sensor and determining the Sun detection threshold.

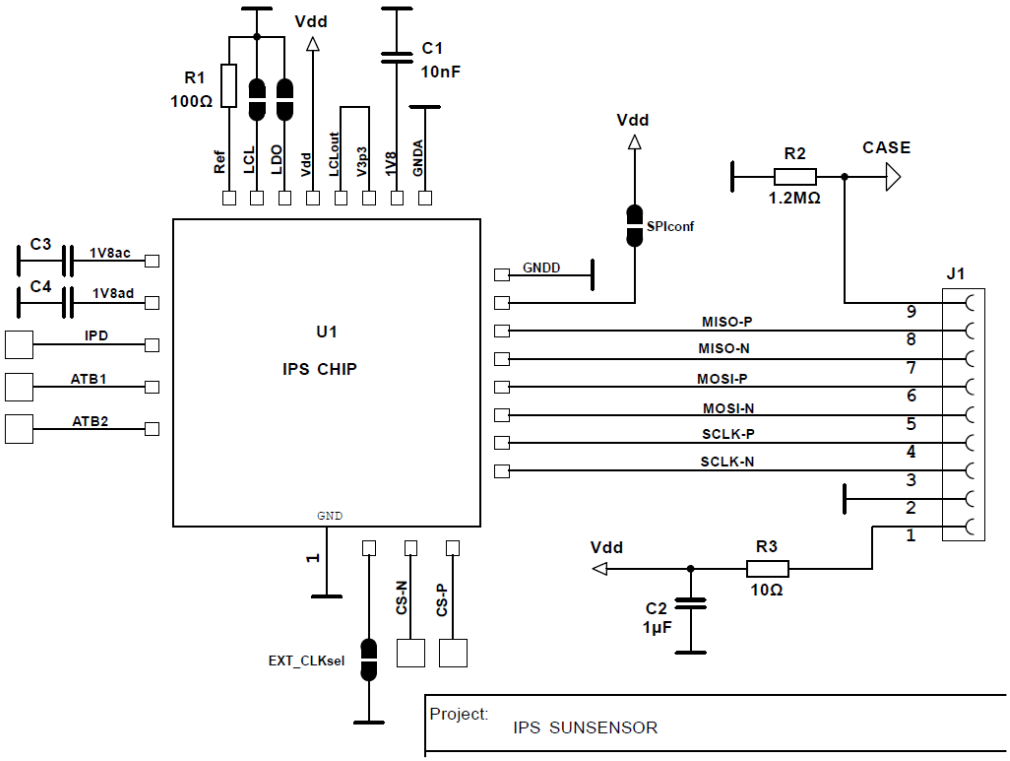

Figure 1 IBIS testbed design

To allow additional tests, two additional bypass capacitors have been foreseen (one for each of the 1.8V LDO's. These capacitors should not be required for the circuit to operate but could prove to be necessary during testing. Last but not least, a chip select activation strap has been implemented allowing to operate several sensors on a single set of digital inputs (which can only be tested by externally wiring for the time being)

All in all, the given schematic leads to a very compact implementation that can be connected by means of a standard 9 pole nano-D connector. The entire sensor is as large as the Lens R&D B.V. MAUS Sunsensor for which the mechanical interfaces are given in Figure 3.

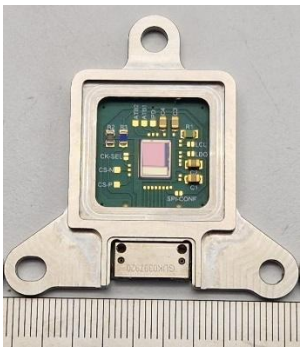

Figure 2 µIBIS

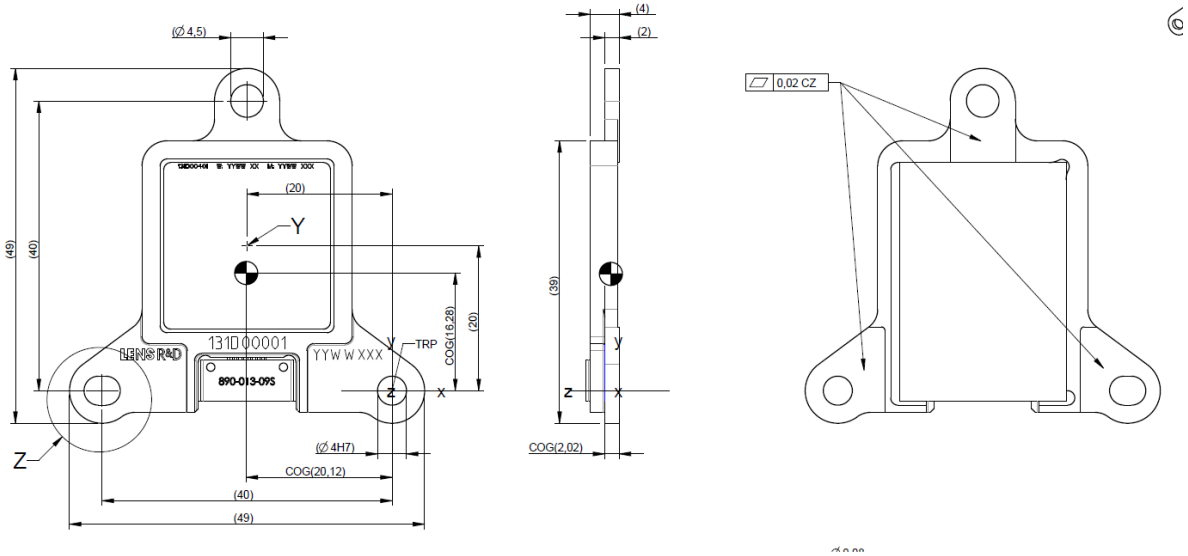

Figure 3 µIBIS mechanical interfaces

Although this is not the final implementation of the IBIS digital Sunsensor foreseen it is significantly smaller than the sensors previously produced by other suppliers.

For the final design of the IBIS (shown in Figure 4) a sensor is foreseen that will look more like the current BiSon sensors. To save costs, the Titanium housing will be replaced with an aluminum housing and the ceramic insert will be replaced by a PEEK insert. This is in line with the regular BiSon version which was taken out of production in 2017 in favor of the current BiSon64-ET.

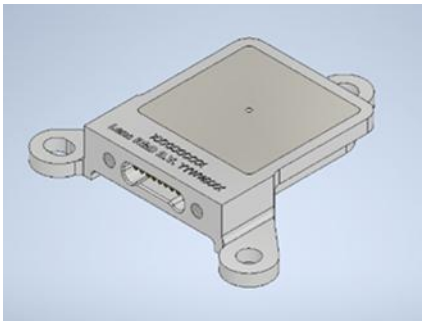

Figure 4 preliminary IBIS design

Radiation tolerance and mitigation

The third major contributor to the power dissipation are the design measures taken to ensure an as high as possible tolerance to cosmic radiation.

Thanks to valuable assistance of ESA experts the design could be optimized to be resistant to cosmic radiation to the largest extend possible.

In general, three types of cosmic radiation are considered to be of importance.

1) Ionizing radiation
2) Non-ionizing radiation
3) Heavy Ions.

Ionizing radiation (total ionizing dose or TID) tends to shift threshold voltages in CMOS circuits causing supply current increases, drift in analogue circuits and eventually circuit failure.
Non-ionizing radiation is known to cause single event upsets like bit flips but also hot pixels or dead pixels

Perhaps the most dangerous radiation is caused by heavy Ions as these particles tend to create conducting trails in the circuit that can lead to a catastrophic latch-up of electronic circuits.

Each of these types of radiation require different mitigation measures that must be incorporated into the design for the final chip to become truly radiation tolerant.

To minimize the effect of TID on the circuits, ESA has financed the design of so-called design against radiation effects (DARE) libraries. The use of these libraries is known to increase the initial power consumption of the circuits produced but also to significantly increase the resistance to ionizing radiation. Whereas the standard TID resistance of a 0.18µm CMOS process has been demonstrated to be in the order of 250krad, the use of the DARE libraries for the IPS+ is expected to increase this to the requested 1Mrad.

Non-Ionizing radiation as caused by protons is known to generate bit flips in memories and digital circuit or signal spikes in analogue circuits. Whereas spikes in the analogue signals can be mitigated by averaging. Bit flips are mitigated by using triple voting redundancy in the digital signal paths at locations that are critical. Triple voting redundancy however means more than triple the amount of electronics that would normally be required and therefore leads to a significant power increase. As these circuits are all in the 1.8V domain this increases the power consumption even more as a nominal 1.5V will have to be reduced by the integrated LDO before the digital circuit is supplied. Nevertheless, the overall power consumption of the total circuit is limited and expected to lead to a manageable thermal design.

Predicted specifications.

Contrary to earlier hopes, delays in the program have led to a situation where no measurement data is available yet. Silicon has been received (after gold coating to increase longevity of the circuits and avoid issues with purple plaque) and assembly of the testbeds is in progress.

Based on simulations we have compiled the following specifications we feel should be obtainable:

Supply voltage	2.5..3.6V (3.3V nominal)	
Power consumption	<100mW	
Field of view	>±64° in diagonal	
accuracy	3.5°	Non-calibrated including albedo errors
	0.5°	Calibrated including albedo errors
	0.2°	target
TID	>1Mrad	At chip level
TNID	>5.10^9 MeV/g	TBC
SEL	>60MeV	
Temperature range	-40°C..+85°C	Of sensor
Sine vibration	40g	*)
Random vibration	34.6g	*)
Shock	3000g	*)
Weight µIBIS	11g	
Weight IBIS	<30g	estimated

Table 2 preliminary specifications

*) values proven for BiSon and MAUS Sunsensors and design is expected to be similar leading to similar resistance values. To save costs, the same qualification levels will be used for the IBIS sensors.

Verified specifications

At this moment in time there are many specifications that cannot be verified yet and testing is mainly limited to functional testing (because no membrane is mounted and the sensor is not fully functional yet) Several test units have been assembled (see Figure 5) and both manufacturing tests and functional testing have delivered significant insights in what could be achieved in the end.

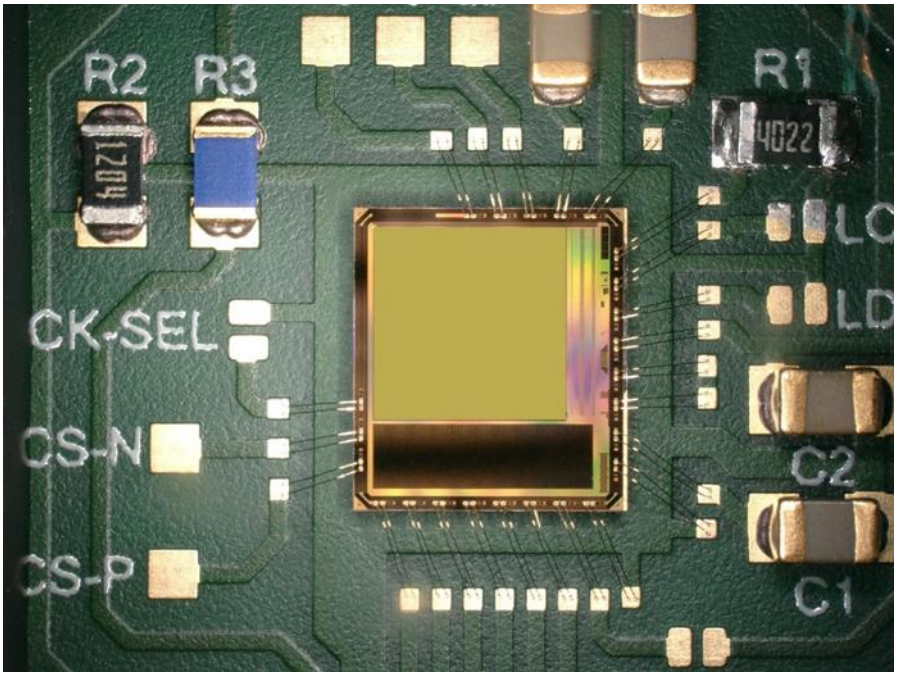

Figure 5 µIBIS testbed after automatic wirebonding

The most important conclusion is that the majority of circuitry seems to be functioning according to specifications and the **cost target for the final product is still deemed achievable**.

Items like field of view and vibration specifications have not been verified yet, but achieving these specifications is highly likely given the resemblance to the BiSon and MAUS products.
Based on assembly tests performed, it is highly likely that an accuracy even higher than the given 3.5°can be achieved without any form of calibration compensation.
It is unclear why, but the measured power consumption is approximately a factor 3 lower than expected (33mW only @3.3V) which reduces the chances to run into thermal problems significantly.
Last but not least, all radiation testing required to optimize the final design for its application must be performed as radiation test results are required to be able to optimize the design for cost effectiveness.

Core circuits like latching digital I/O, current limiter, low dropout regulators, watchdog timer, reference generator, detector array and digital signal processing are all functioning within expectation.
Some circuits still need to be tested, but it is clear that, despite all the verified functionality, this chip cannot be used to build a real functional Sunsensor.

Due to a wiring mistake in the imager control bus, instead of selecting one line to process, the digital processer addresses all lines but the one that should have been selected.
This means that a new version of the chip will have to be produced for which this on-chip wiring error is corrected.

Currently this drives the further development of the system as the chip will have to be manufactured again, gold plated, diced and assembled in a number of testbeds for further testing.

Planning

The further development of the IBIS sensor will take a number of steps to complete.

1. Redesign the current chip and produce new samples
2. Assemble µIBIS sensors without membrane for functional and radiation testing
3. Perform radiation tests
    a. Total Ionizing dose
    b. Proton
    c. Heavy Ion
4. Assemble µIBIS including test membrane to verify measurement accuracy
5. Modify at least one of the available calibration setups to be able to calibrate the sensors correctly
6. Commission and verify all required test setups and equipment
7. Design the IBIS sensor on basis of obtained radiation results.
8. Perform environmental qualification on IBIS and µIBIS sensors.

At this moment in time, it is foreseen to perform the radiation testing and further environmental qualification more or less in parallel so as to speed up the overall project completion. This in turn leads to a goal to have the full qualification finished before the end of 2026. Given the content of all activities combined this is challenging but seems manageable if the redesign and re-run of the chip can be completed within 2025.

Full qualification is by no means expected to lead to an end to the production optimization activities as automated known good die testing will be an essential part of the equation that will lead to cost effective sensor production.

Conclusions

A radiation hardened single chip true digital Sunsensor is under development at Lens R&D B.V. This development not only builds on many years of pre-developments as performed within ESA frame by companies like Galileo Avionica and TNO, but also on more than a decade of design for produceability developments at Lens R&D B.V. and its supply partners.

Strategic partnerships with critical partners and suppliers, the availability of a qualified housing integrated wirebondable connector and a dedicated radiation hardened silicon chip provide all the ingredients needed to lead to a commercially successful product that can be cost effectively manufactured at scales required by current and future large satellite constellations.

Space grade Commercial Of The Shelf availability of a radiation hardened true digital Sunsensor will be the crown on a 30 year long development trajectory and a clear sign that providing high reliability solutions for even something as simple as a Sunsensor can be very challenging.

Although developments for digital Sunsensors have been running for decades within various ESA funded programs, the current program is the first program expected to lead to a commercially attractive fully qualified solution. Once qualified this solution is expected to have a major impact on the market for high reliability Sunsensors worldwide and will ensure European independence for many years to come.

References:

1. de Boom, C.W. et all, *ESA GNC.* **2011**, *Mini-DSS: MINIATURIZED HIGH-PRECISION SUN-ANGLE MEASUREMENT;* 2. *de Boer, B.M.. et all, ESA ICSO 2012, MiniDSS: a low-power and high-precision miniaturized digital Sun sensor*